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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	9

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,882	HO ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 8(a) Number 801, 832, and 834. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 9 Number 910. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 910b" on Page 16 Line 10. A proposed drawing correction or corrected

drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 3, 4, 5, 11, 12, 13, 14, 20, 21, 22, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,591,324 to Chen et al. ("Chen"), US Patent Number 6,260,092 to Story et al. ("Story"), and the specification of the present application.

6. In reference to Claim 1, Chen teaches a computer system including a circuit board (See Figure 2 and Column 3 Lines 29-30); a first slot and a second slot coupled to said circuit board wherein said first slot includes a first connector and said second slot includes a second connector (See Figure 2 Numbers 105 and 130 and Column 3 Lines 30-44); a primary hot swap controller (See Figure 2 Number 120 and Column 4 Lines 40-47) having a first means for simultaneously turning on/off a first plurality of switches (See Figure 2 Numbers 114 and 120, Column 3 Lines 49-52, Column 4 Lines

4-15, and Column 4 Lines 61-63), and a second means for driving signal lines connected to the connector-pins (See Figure 2 Numbers 116 and 118, Column 3 Lines 39-48, and Column 4 Lines 13-15); a backup hot swap controller (See Figure 2 Number 120 and Column 4 Lines 48-49) having a fourth means for simultaneously turning on/off a second plurality of switches (See Figure 2 Numbers 114 and 120, Column 3 Lines 49-52, Column 4 Lines 4-15, and Column 4 Lines 61-63), and a fifth means for driving signal lines connected to the connector-pins (See Figure 2 Numbers 116 and 118, Column 3 Lines 39-48, and Column 4 Lines 13-15); during normal operation of said computer system said first means turns on said first plurality of switches such that said second means drives said signal lines connected to said the connector-pins and said fourth means turns off said second plurality of switches (See Column 4 Lines 40-46); and during backup operation of said computer system, said first means turns off said first plurality of switches and said fourth means turns on said second plurality of switches such that said fifth means drives said signal lines connected to the connector-pins (See Column 4 Lines 57-66). The device of Chen conforms to the Compact PCI Hot-Swap Specification (See Column 1 Lines 56-61 and Column 3 Lines 27-28). As evidenced by the specification of the present application, which discusses compact PCI in its conventional use, Chen inherently includes the first and second connectors having a column and row arrangement of connector-pins (See Figure 3); said first connector including first, second, and third connector-pins (See Figures 3 and 9); said second connector including fourth, fifth, and sixth connector-pins (See Figures 3 and 9); first, second, third, fourth, fifth, and sixth signal lines connected to said first through sixth

connector-pins, respectively (See Figures 6a and 6b). Chen does not teach a third means for storing a status information of said signal lines; a fifth means for storing a status information of said signal lines; and driving said signal lines connected to said first, second, fourth, and fifth connector-pins according to said status information stored in said fifth means. Story teaches an input register that stores data as it passes through the interface and later transmits said data onto the bus (analogous to the third and fifth storage means for storing a status information of said signal lines) (See Column 4 Lines 27-31); and driving the signal lines according to the status information stored in the register (See Column 4 Lines 22-26 and 29-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 1, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

7. In reference to Claim 2, Chen and Story teach the limitations as applied to Claim 1 above. Chen further teaches a first communication control circuit (See Column 4 Lines 25-39); said second means connected to said first plurality of switches and to said first means (See Figure 2); said first means connected to activation terminals of said first switches via a first control line so as to simultaneously turn on/off said first plurality of switches (See Column 4 Lines 4-11 and 61-63); said communication control circuit coupled to said first means (See Column 5 Lines 4-8 and 22-24); and said first through sixth connector-pins connected to said second means via said signal lines and through

respective ones of said first plurality of switches (See Figure 2, Column 51-55, Column 4 Lines 13-15, and Column 5 Lines 59-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 2, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

8. In reference to Claim 3, Chen and Story teach the limitations as applied to Claim 2 above. Chen further teaches said fifth means connected to said second plurality of switches and to said fourth means (See Figure 2); said fourth means connected to respective activation terminals of said second switches via a second control line so as to simultaneously turn on/off said first plurality of switches (See Column 4 Lines 4-11 and 61-63); said fourth means having a communication link with said first communication control circuit (See Column 5 Lines 4-8 and 22-24); and said first through sixth connector-pins connected to said fifth means via said signal lines and through respective ones of said second plurality of switches (See Figure 2, Column 51-55, Column 4 Lines 13-15, and Column 5 Lines 59-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 3, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

9. In reference to Claim 4, Chen and Story teach the limitations as applied to Claim 1 above. Chen further teaches that said first means includes a circuit that controls arbitration by determining whether the switches are to be turned on or off and thus arbitrating which card is connected to the bus (See Column 4 Lines 4-15 and 59-64); said second means including a core control circuit (See Figure 2 Number 118). Chen does not teach that said third means includes a first register. Story teaches an input register that stores data as it passes through the interface and later transmits said data onto the bus (See Column 4 Lines 27-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 4, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

10. In reference to Claim 5, Chen and Story teach the limitations as applied to Claim 1 above. Chen further teaches that said fourth means includes a second communication circuit (See Column 5 Lines 4-8 and 22-24). Chen does not teach that said fifth means includes a second register. Story teaches an input register that stores data as it passes through the interface and later transmits said data onto the bus (See Column 4 Lines 27-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting

in the invention of Claim 5, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

11. In reference to Claim 11, Chen and Story teach the limitations as applied to Claim 2 above. Chen further teaches that wherein said first communication control circuit is connected to said first means via a plurality of control lines (See Column 4 Lines 34-39 and Column 5 Lines 4-24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 11, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

12. In reference to Claim 12, Chen and Story teach the limitations as applied to Claim 1 above. Because the device of Chen is a Compact PCI device (See Column 1 Lines 56-61 and Column 3 Lines 27-28 of Chen), and because Compact PCI devices have a plurality of lines, as evidenced in the present application (See Figure 3), it is inherent that the device of Chen would connect the first means to the second means by a plurality of control lines.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 12, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

13. In reference to Claim 13, Chen and Story teach the limitations as applied to Claim 1 above. Because the device of Chen is a Compact PCI device (See Column 1 Lines 56-61 and Column 3 Lines 27-28 of Chen), and because Compact PCI devices have a plurality of lines, as evidenced in the present application (See Figure 3), it is inherent that the device of Chen would connect the fourth means to the fifth means by a plurality of signal lines.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 13, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

14. In reference to Claim 14, Chen teaches a hot swappable computer system including a circuit board (See Figure 2 and Column 3 Lines 29-30); said circuit board having a slot with a first connector (See Figure 2 Numbers 105 and 130 and Column 3 Lines 30-44); a primary hot swap controller having a core control circuit (See Figure 2 Number 118) having a plurality of first switches (See Column 2 Lines 15-17), a first communication control circuit (See Column 4 Lines 25-39), a circuit that controls arbitration by determining whether the switches are to be turned on or off and thus arbitrating which card is connected to the bus (See Column 4 Lines 4-15 and 59-64); said core control circuit connected to said plurality of first switches and said arbitration control circuit (See Figure 2); said arbitration control circuit connected to said first

communication control circuit and to activation terminals of said first switches via a common control line such that said first switches are turned on/off simultaneously by said arbitration control circuit (See Column 4 Lines 4-11 and 61-63 and Column 5 Lines 4-8 and 22-24); a backup hot swap controller (See Figure 2 Number 120 and Column 4 Lines 48-49) having a plurality of second switches (See Column 2 Lines 15-17), and a second communication control circuit (See Column 4 Lines 25-39); said second communication control circuit connected to respective activation terminals of said second switches via a common control line such that said second switches are turned on/off simultaneously by said second communication control circuit (See Column 5 Lines 4-8 and 22-24); and said second communication control circuit has a communication link with said first communication control circuit (See Column 4 Lines 25-39); wherein during a normal operation of said computer system, said primary hot swap controller drives the signal lines (See Column 4 Lines 40-47); and during backup operation of said computer system, said backup hot swap controller drives the signal lines (See Column 4 Lines 57-64). The device of Chen conforms to the Compact PCI Hot-Swap Specification (See Column 1 Lines 56-61 and Column 3 Lines 27-28). As evidenced by the specification of the present application, which discusses compact PCI in its conventional use, Chen inherently includes the first connector having a column and row arrangement of connector-pins (See Figure 3); said first connector including first, second, and third connector-pins (See Figures 3 and 9); and first second and third signal lines connected to said first, second, and third connector-pins (See Figures 6a and 6b). Chen does not teach that the primary hot swap controller includes a first

register; the backup hot swap controller has a second register; said second register connected to said second switches and said second communication control circuit; and during a backup operation of said computer system said backup hot swap controller drives said first, second, and third signal lines according to a status of said respective signal lines stored in said second register. Story teaches an input register that stores data as it passes through the interface and later transmits said data onto the bus (See Column 4 Lines 27-31); and driving the signal lines according to the status information stored in the register (See Column 4 Lines 22-26 and 29-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 14, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

15. In reference to Claim 20, Chen teaches the limitations as applied to Claim 14 above. Chen does not teach that said first register stores a status of said first, second, and third signal lines. Story teaches that the register stores a data representation containing the states of all signals that must be driven and information about whether to drive and to what state for signals that may be driven (See Column 4 Lines 21-31)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 19, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

16. In reference to Claim 21, Chen and Story teach the limitations as applied to Claim 14 above. Chen further teaches that wherein said first arbitration control circuit is connected to said first communication control circuit via a plurality of control lines (See Column 4 Lines 34-39 and Column 5 Lines 4-24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 21, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

17. In reference to Claim 22, Chen and Story teach the limitations as applied to Claim 14 above. Because the device of Chen is a Compact PCI device (See Column 1 Lines 56-61 and Column 3 Lines 27-28 of Chen), and because Compact PCI devices have a plurality of lines, as evidenced in the present application (See Figure 3), it is inherent that the device of Chen would connect the arbitration control circuit to the core control circuit by a plurality of control lines.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 22, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

18. In reference to Claim 23, Chen and Story teach the limitations as applied to Claim 14 above. Because the device of Chen is a Compact PCI device (See Column 1 Lines 56-61 and Column 3 Lines 27-28 of Chen), and because Compact PCI devices have a plurality of lines, as evidenced in the present application (See Figure 3), and because the register of Story provides an interface between a data source and a bus (See Column 4 Lines 27-31 of Story), it is inherent that said second communication control circuit is connected to said second register via a plurality of signal lines.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 23, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

19. In reference to Claim 24, Chen teaches a backup hot swap controller (See Figure 2 Number 120 and Column 4 Lines 48-49) including a circuit board (See Figure 2 and Column 3 Lines 29-30); said circuit board having a slot with a first connector (See Figure 2 Numbers 105 and 130 and Column 3 Lines 30-44); said circuit board having a plurality of switches (See Column 2 Lines 15-17); said switches connected to the connector-pins via signal lines (See Column 2 Lines 15-17); a communication control circuit (See Column 4 Lines 25-39); and said communication control circuit connected to respective activation terminals of said switches and having a common control for simultaneously turning on/off said plurality of switches (See Column 5 Lines 4-8 and 22-24). The device of Chen conforms to the Compact PCI Hot-Swap Specification (See

Column 1 Lines 56-61 and Column 3 Lines 27-28). As evidenced by the specification of the present application, which discusses compact PCI in its conventional use, Chen inherently includes connectors having a column and row arrangement of connector-pins (See Figure 3); first ones of said connectors of said slots having first, second, and third connector-pins (See Figures 3 and 9); and first second and third signal lines connected to said first, second, and third connector-pins (See Figures 6a and 6b). Chen does not teach a register for storing status information of said signal lines; said register connected to said plurality of switches; the communication control circuit connected to said register; and wherein during the period when said communication control circuit turns on said switches, said register drives said signal lines connected to said first, second, and third connector pins according to said status stored in said register. Story teaches an input register that stores data as it passes through the interface and later transmits said data onto the bus (See Column 4 Lines 27-31); and driving the signal lines according to the status information stored in the register (See Column 4 Lines 22-26 and 29-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen with the register of Story, resulting in the invention of Claim 24, in order to keep the data in sync with the bus clock (See Column 4 Lines 32-33 of Story).

20. Claims 6, 7, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Story as applied to Claim 3 above, and further in view of the US Patent Number 6,324,485 to Ellis ("Ellis").

21. In reference to Claim 6, Chen and Story teach the limitations as in Claims 3 and 14 above. Chen and Story do not teach that the communication link connecting said first communication control circuit and said fourth means comprise an asynchronous communication link. Chen teaches that the communications line may be of any sort (See Column 4 Line 30). Ellis teaches the use of a source-synchronous communication link in which data is synchronous to the source, but asynchronous to the destination (See Column 2 Lines 10-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Chen and Story with the source-synchronous bus of Ellis, resulting in the invention of Claim 6, because Chen teaches that the communications line may be of any sort (See Column 4 Line 30 of Chen); and because a source-synchronous bus more easily creates and maintains accurate clock to data relationships (See Column 2 Lines 13-15 of Ellis).

22. In reference to Claim 7, Chen, Story, and Ellis teach the limitations as in Claim 6 above. Chen and Story do not teach that said asynchronous communication link includes a data line and a clock line. Ellis teaches that a source-synchronous bus includes a data line and a clock line (See Column 2 Lines 10-12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Chen and Story with the source-synchronous bus of Ellis, resulting in the invention of Claim 7, because Chen teaches that the communications line may be of any sort (See Column 4 Line 30 of Chen); and because a source-synchronous bus more easily creates and maintains accurate clock to data relationships (See Column 2 Lines 13-15 of Ellis).

23. In reference to Claim 15, Chen and Story teach the limitations as in Claim 14 above. Chen and Story do not teach that the communication link connecting said first and second communication control circuits comprise an asynchronous communication link. Chen teaches that the communications line may be of any sort (See Column 4 Line 30). Ellis teaches the use of a source-synchronous communication link in which data is synchronous to the source, but asynchronous to the destination (See Column 2 Lines 10-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Chen and Story with the source-synchronous bus of Ellis, resulting in the invention of Claim 15, because Chen teaches that the communications line may be of any sort (See Column 4 Line 30 of Chen); and because a source-synchronous bus more easily creates and maintains accurate clock to data relationships (See Column 2 Lines 13-15 of Ellis).

24. In reference to Claim 16, Chen, Story, and Ellis teach the limitations as in Claim 15 above. Chen and Story do not teach that said asynchronous communication link includes a data line and a clock line. Ellis teaches that a source-synchronous bus includes a data line and a clock line (See Column 2 Lines 10-12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Chen and Story with the source-synchronous bus of Ellis, resulting in the invention of Claim 16, because Chen teaches that the communications line may be of any sort (See Column 4 Line 30 of Chen); and because a source-synchronous bus more easily creates and maintains accurate clock to data relationships (See Column 2 Lines 13-15 of Ellis).

25. Claims 8, 9, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Story as applied to Claim 3 and 14 above, and further in view of the PCI Local Bus Specification, Revision 2.1 ("PCI Specification").

26. In reference to Claim 8, Chen and Story teach the limitations as in Claim 3 above. Chen and Story do not teach that the communication link connecting said first communication control circuit and said fourth means comprise a synchronous communication link. Chen teaches that the communications line may be of any sort (See Column 4 Line 30). The PCI Specification teaches that a PCI bus is a synchronous bus (See Page 4, Section 1.5, Subsection "High Performance, Bullet 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Chen and Story with a PCI communications link, resulting in the invention of Claim 8, because Chen teaches that the communications line may be of any sort (See Column 4 Line 30 of Chen); and because a PCI bus provides high performance, low cost, ease of use, longevity, reliability, and flexibility (See Pages 4-5 of the PCI Specification).

27. In reference to Claim 9, Chen, Story, and the PCI Specification teach the limitations as in Claim 8 above. Chen and Story do not teach that said synchronous communication link includes a plurality of data lines, a plurality of control lines, and a select/strobe control line. The PCI Specification teaches that a PCI bus has a plurality of data lines, a plurality of control lines, and IDSEL, DEVSEL#, and clock lines (analogous to the select/strobe control line) (See Page 7, Figure 2-1 of the PCI Specification).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Chen and Story with a PCI communications link, resulting in the invention of Claim 9, because Chen teaches that the communications line may be of any sort (See Column 4 Line 30 of Chen); and because a PCI bus provides high performance, low cost, ease of use, longevity, reliability, and flexibility (See Pages 4-5 of PCI Specification).

28. In reference to Claim 17, Chen and Story teach the limitations as in Claim 14 above. Chen and Story do not teach that the communications link connecting said first and second communication control circuits comprise a synchronous communication link. Chen teaches that the communications line may be of any sort (See Column 4 Line 30). The PCI Specification teaches that a PCI bus is a synchronous bus (See Page 4, Section 1.5, Subsection "High Performance, Bullet 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Chen and Story with a PCI communications link, resulting in the invention of Claim 17, because Chen teaches that the communications line may be of any sort (See Column 4 Line 30 of Chen); and because a PCI bus provides high performance, low cost, ease of use, longevity, reliability, and flexibility (See Pages 4-5 of the PCI Specification).

29. In reference to Claim 18, Chen, Story, and the PCI Specification teach the limitations as in Claim 17 above. Chen and Story do not teach that said synchronous communication link includes a plurality of data lines, a plurality of control lines, and a select/strobe control line. The PCI Specification teaches that a PCI bus has a plurality of data lines, a plurality of control lines, and IDSEL, DEVSEL#, and clock lines (analogous to the select/strobe control line) (See Page 7, Figure 2-1 of the PCI Specification).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Chen and Story with a PCI

communications link, resulting in the invention of Claim 18, because Chen teaches that the communications line may be of any sort (See Column 4 Line 30); and because a PCI bus provides high performance, low cost, ease of use, longevity, reliability, and flexibility (See Pages 4-5 of PCI Specification).

30. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Story as applied to Claims 2 and 14 above, and further in view of US Patent Number 6,145,099 to Shindou ("Shindou").

31. In reference to Claim 10, Chen and Story teach the limitations as applied in Claim 2 above. Chen and Story do not teach that wherein during every programmed interval of said normal operation, the status of said signal lines connected to said first through sixth connector-pins are transmitted from said first communication control circuit to said fourth means and stored in said fifth means. Shindou teaches a device that continuously monitors signals and saves a copy of the signals that are then transmitted to another device (See Figure 5 and Column 7 Lines 30-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen and Story with the bus signal copying and storage system of Shindou, resulting in the invention of Claim 10, in order to observe internal states and operations of the bus and allow the information to be sent to another system for debugging purposes (See Column 4 Lines 56-58 of Shindou).

32. In reference to Claim 19, Chen and Story teach the limitations as applied in Claim 14 above. Chen and Story do not teach that wherein during every programmed interval of said normal operation, the status of said signal lines connected to said first through third connector-pins are transmitted from said first communication control circuit to said second communication control circuit and stored in said second register. Shindou teaches a device that continuously monitors signals and saves a copy of the signals that are then transmitted to another device (See Figure 5 and Column 7 Lines 30-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Chen and Story with the bus signal copying and storage system of Shindou, resulting in the invention of Claim 19, in order to observe internal states and operations of the bus and allow the information to be sent to another system for debugging purposes (See Column 4 Lines 56-58 of Shindou).

Information Disclosure Statement

33. The information disclosure statement filed 26 July 2001 fails to comply with 37 CFR 1.98(a)(1), which requires a list of all patents, publications, or other information submitted for consideration by the Office. It has been placed in the application file, but the information referred to therein has not been considered.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Number 6,026,458 to Rasums et al. ("Rasums") is directed to hot swapping of devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4:30), Alt. Fridays (7-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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